AMENDMENTS

In The Claims:

Claims 1-7. (cancelled)

Claim 8. (original) A method of fabricating a non-volatile memory cell, comprising:

forming a bottom dielectric layer, a charge trapping layer, a first top dielectric layer and a mask layer on a substrate sequentially;

etching the mask layer for forming a first trench exposing a portion of the first top dielectric layer;

forming a plurality of first spacers on sidewalls of the first trench;

using the first spacers as an etching mask and etching the first top dielectric layer and the charge trapping layer for forming a second trench;

removing the first spacers;

forming a second top dielectric layer over the substrate, covering surfaces of the second trench and the first trench;

forming a conductive layer in the first trench and the second trench;

removing the conductive layer and the second top dielectric layer outside of the first trench and the second trench for exposing the mask layer;

removing the exposed mask layer;

using the conductive layer as a mask, removing the first top dielectric layer, the charge trapping layer and the bottom dielectric layer for forming a stacked structure; and

forming source/drain regions in the substrate adjacent to edges of the stacked structure.

Claim 9. (original) The method of fabricating a non-volatile memory cell of claim 8, before forming the source/drain regions, further comprising:

forming a plurality of lightly doped regions in the exposed substrate; and

forming a plurality of second spacers on the sidewalls of the stacked structure.

Claim 10. (original) The method of fabricating a non-volatile memory cell of claim 8, wherein the step of forming the bottom dielectric layer comprises forming a silicon oxide layer on a surface of the substrate by a thermal oxidation process.

Claim 11. (original) The method of fabricating a non-volatile memory cell of claim 8, wherein the step of forming the charge trapping layer comprises forming a silicon nitride layer on the bottom dielectric layer by a chemical vapor deposition process.

Claim 12. (original) The method of fabricating a non-volatile memory cell of claim 8, wherein the material of the mask layer comprises silicon nitride.

Claim 13. (original) The method of fabricating a non-volatile memory cell of claim 8, wherein the material of the first spacers comprise polysilicon.

Claim 14. (original) The method of fabricating a non-volatile memory cell of claim 8, wherein the material of conductive layer comprises polysilicon.

Claim 15. (original) The method of fabricating a non-volatile memory cell of claim 8, wherein the material of the charge trapping layer is selected from a group consisting of silicon nitride, tantalum oxide, $SrTiO_3$ and hafnium oxide.

Claim 16. (original) The method of fabricating a non-volatile memory cell of claim 8, wherein the material of the first top dielectric layer and the second top dielectric layer comprises silicon oxide.

Claim 17. (original) The method of fabricating a non-volatile memory cell of claim 8, wherein the step of removing the conductive layer and the second top dielectric layer outside of the first trench and the second trench is a chemical mechanical polishing process or an etch-back process.

Claim 18. (original) The method of fabricating a non-volatile memory cell of claim 8, wherein the step of removing the mask layer comprises dry etching.